Amendments to the Claims

1. (CURRENTLY AMENDED) A converter for converting an input digital signal ~~(1)~~ into an output digital signal (2), said converter comprising:

- a set of shift registers ~~(121, 122, 143, 144)~~ able to contain samples of the input or output digital signal,

- a calculation unit able to supply a shift signal ~~(4)~~ to said set of registers and comprising:

- a first storage unit ~~(51)~~ able to contain a value of a conversion ratio or of its inverse, so that the stored value is between 0 and 1,

- a second storage unit ~~(52)~~ able to contain, at a cycle time i+1, i being an integer, a future signal ~~(8)~~ equal to a sum of a current signal ~~(7)~~ contained in the second unit at a cycle time i and of the content of the first storage unit,
the shift signal resulting from an exclusive OR function ~~(54)~~ between a most significant bit of the current signal ~~(71)~~ and a most significant bit of the future signal ~~(81)~~.

2. (CURRENTLY AMENDED) A calculation unit able to supply a shift signal ~~(4)~~ to a set of shift registers ~~(121, 122, 143, 144)~~ of a converter converting an input digital signal ~~(1)~~ into an output digital signal ~~(2)~~ and comprising:

- a first storage unit ~~(51)~~ able to contain a value of a conversion ratio or of its inverse, so that the stored value is between 0 and 1,

- a second storage unit ~~(52)~~ able to contain a cycle time i+1, i being an integer, a future signal ~~(8)~~ equal to a sum of a current signal ~~(7)~~ contained in the second unit at a cycle time i and of the content of the first storage unit,
the shift signal resulting from an exclusive OR function ~~(54)~~ between a most significant bit of the current signal ~~(71)~~ and a most significant bit of the future signal ~~(81)~~.

3. (CURRENTLY AMENDED) A calculation unit as claimed in claim 2, comprising an initialization circuit ~~(55)~~ able to load an initialization signal ~~(56)~~ into the second storage unit ~~(52)~~ at the start of a processing of the input digital signal ~~(1)~~.

4. (ORIGINAL) A digital television receiver comprising a converter as claimed in claim 1.

5. (CURRENTLY AMENDED) A method of converting an input digital signal ~~(1)~~ into an output digital signal ~~(2)~~, said method comprising a calculation step able to supply a shift signal to a set of shift registers, itself comprising the substeps of:

- storage of a value of a conversion ratio or of its inverse, so that the value stored is between 0 and 1,

- addition or subtraction of the value previously stored to or from a current signal initially equal to an initialization signal, resulting from a future signal,

- exclusive OR between a most significant bit of the current signal and a most significant bit of the future signal.

6. (ORIGINAL) A computer program able to implement the signal conversion method as claimed in claim 5, when said program is executed by a processor.